## ABSTRACT OF THE DISCLOSURE

A reconfigurable processor architecture. A reconfigurable processor is an array of a multiplicity of various functional elements, between which the interconnections may be programmably configured. The inventive processor is implemented on a single substrate as a network of clusters of elements. Each cluster includes a crossbar switching node to which a plurality of elements is connected via ports. Additional ports on the crossbar switching node connect to the switching nodes of nearest neighbor clusters. The crossbar switching nodes allow pathways to be programmably set between any of the ports, and any pathway may be set to be either registered or unregistered. The use of clusters of processing elements allows complete freedom of local connectivity for effective configuration of many different processing functions. Wide area interconnection is more restricted, but, since it is less used, does not significantly restrict configurability. The inventive processor thus provides 1) high configurability with a low cost of switching network overhead; 2) constant clock speed, independent of configuration; and 3) very high clock speed since all communication is local or nearest neighbor.